

REMARKS

Claims 1, 2, and 4-12 are pending in the present application. Claim 1 is amended above. New claim 13 is added. No new matter is added by the claim amendments or new claim. Entry is respectfully requested.

Claims 1, 2, and 4-12 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Laparra *et al.* (U.S. 6,319,796 - hereinafter "Laparra") in view of Park *et al.* (U.S. 6,326,282 - hereinafter "Park") and Shin *et al.* (U.S. 6,184,077 - hereinafter "Shin"). It is requested that this rejection be reconsidered and removed in view of the following remarks.

It is respectfully submitted that a *prima facie* case of obviousness has not been established in the present application, or is improper. In particular, there is no motivation to combine the teachings of the Laparra reference with those of the Park or Shin reference, nor is there a suggestion of the desirability of such a combination. In addition, there is no reasonable expectation of success in their combined teachings. The Laparra coating 40b is applied to the underlying insulating layer 40a in order to reduce thickness unevenness (Laparra, column 5, line 4 - column 6, line 10). In this manner, the degree of planarity during subsequent planarization operations is increased (Laparra, column 6, lines 11-17). To accomplish this, Laparra cites high-density plasma (HDP) deposition of silica-based material, and low-pressure chemical vapor deposition (LPCVD) of a dielectric including TEOS as suitable materials for the coating 40b (Laparra, column 5, lines 50-57).

The "HTO" layers discussed in Park and Shin are unable to accomplish this, since the properties of an HTO layer are such that the HTO layer closely matches the unevenness of an underlying layer. Support for this position is provided in the following articles, copies of which are attached to this Amendment:

"A Comparison of Planarization Properties of TEOS and SiH<sub>4</sub> PECVD Oxides", by Magnella, *et al.*, V-MIC Conference, June 13-14, 1988, pgs. 366-373; and

“Sticking Coefficient as a Single Parameter to Characterize Step Coverage of SiO<sub>2</sub> Processes”, by Cheng *et al.*, V-MIC Conference, June 12-13, 1990, pgs. 404-406.

Magnella *et al.*, at page 366, last paragraph, teaches that “CVD silane deposition above 600C is typically very conformal”. This is supported by Cheng *et al.* at page 405, second paragraph, which states that the sticking coefficient of silane (0.26) is very high as compared to TEOS (0.045), which means that CVD silane deposition is very conformal. Since CVD silane deposition is very conformal, the application of an HTO layer would not reduce thickness unevenness in the manner specified by Laparra.

If an HTO layer were applied as the coating layer 30b of Laparra, the surface unevenness of coating layer 40b would be the same as that of the underlying insulating layer 40a. Thus, a reduction in thickness unevenness would not be achieved. Accordingly, one of ordinary skill in the art would not be motivated to combine the teachings of Park and/or Shin with Laparra, since an applied HTO layer would be ineffective in reducing thickness unevenness. Accordingly, reconsideration and removal of the rejection are respectfully requested.

The present invention as claimed in independent claim 1 is directed to a method for providing trench isolation in a semiconductor device. An etching mask pattern is formed on a semiconductor substrate to expose a predetermined region of the semiconductor substrate. The exposed semiconductor substrate is then etched, using the etching mask pattern as an etching mask, to form a trench. An insulating layer is formed over the trench and nearby regions, the insulating layer filling the trench. A high-temperature oxide (HTO) layer is provided on the insulating layer, the HTO layer being formed at a temperature of 700C to 800C using a silane-based source gas. In this manner the underlying insulating layer is densified during formation of the HTO layer. The HTO layer and the insulating layer are planarly etched down to a top surface of the etching mask pattern to form a device isolation layer pattern in the trench. The exposed etching mask pattern is then removed. (emphasis added).

In this manner, the method of the present invention as claimed in claim 1 provides for densification of the insulating layer (see for example, reference 23 of FIG. 1F), during formation of the HTO layer (reference 24 of FIG. 1F) at a temperature of 700C - 800C using a silane-based source gas. Accordingly, there is no need to perform a subsequent, additional annealing process in order to densify the underlying insulating layer, which otherwise could lead to a number of process limitations, as specified in the present application as filed at page 2, lines 2 - 23. By virtue of the fact that a silane-based source gas is used to form the high-temperature oxide (HTO) layer, penetration of carbon into adjacent active regions of the device is avoided, and therefore, densification of the underlying insulating layer occurs without adversely affecting nearby active regions.

The current Office Action, at page 4, paragraph 1, suggests that former claim 1 failed to specify the manner in which the HTO layer is formed "outside of temperature constraints". For this reason, applicants' earlier arguments related to the ineffectiveness of an LP-TEOS-based layer as a replacement for the claimed HTO layer were considered "non-persuasive".

It is respectfully submitted that claim 1 is therefore amended above to state that the HTO layer is further "formed ... using a silane-based source gas", for example, silane ( $\text{SiH}_4$ ) or dichlorosilane ( $\text{SiH}_2\text{Cl}_2$ ) source gas, in order to further differentiate the claimed HTO process step from the LP-TEOS process step. It is believed that this limitation clearly distinguishes the HTO process.

As stated in the previous response filed by the applicants on June 26, 2003, the applicants respectfully disagree with the position taken in the Office Action that Shin and Park teach that the HTO and LP-TEOS processes are interchangeable, and should therefore be considered as "art equivalent layers" (Office Action of March 26, 2003, page 3, paragraph 4). In particular, the applicants respectfully submit that the LP-TEOS process would be ineffective when applied to the presently claimed method, since it would result in the penetration of carbon in adjacent active regions of the device. In support of the applicants' position, the following

discussion relating to the distinctions between the LP-TEOS and HTO processes is repeated from the earlier Response filed by the applicants on June 26, 2003.

Chemical Vapor Deposition (CVD) processes, used for forming a silicon dioxide layer, can be classified as atmospheric-pressure-CVD (AP-CVD) and low-pressure CVD (LP-CVD), in terms of the pressure under which the process takes place. AP-CVD is performed at low temperature, but has poor step coverage. LP-CVD is performed at high temperature, and has heightened step coverage. When plasma is used in the LP-CVD process, for example in the plasma-enhanced-CVD process (PE-CVD), deposition can be performed at a lower process temperature.

The composition of the resulting silicon oxide formed as a result of the various CVD processes described above can vary according to process source gasses used, process pressure and process temperature. For example, the LP-TEOS-based layer mentioned in Park and Shin, refers to a silicon oxide layer, formed in the LP-CVD process, using TEOS as a source gas. The LP-TEOS formation process is performed at a high temperature, because the LP-CVD deposition process is used.

On the other hand, the "HTO layer", stated in claim 1 of the present invention, is a silicon oxide layer that is formed at a high temperature, using a silane-based source gas, for example, of silane ( $\text{SiH}_4$ ) gas or dichlorosilane ( $\text{SiH}_2\text{Cl}_2$ ) gas.

Based on the above, it is apparent that both the LP-TEOS-based layer and HTO-based layer are representative of silicon oxide layers formed using a LP-CVD process, and are therefore formed at a high temperature. However, the resulting oxide layers are entirely different in composition, since the source gases used for in their formation are different. For this reason, claim 1 specifically refers to an "HTO layer", namely, a "high-temperature *oxide*" layer, that is, specifically, a term of art that referring to an oxide layer formed using a silane ( $\text{SiH}_4$ ) or dichlorosilane ( $\text{SiH}_2\text{Cl}_2$ ) source gas,

and not merely to just *any* oxide layer that is formed by high temperature, *i.e.* any high-temperature *process* that results in oxide layer formation, for example TEOS.

It is further submitted that replacement of the HTO layer with an LP-TEOS layer for the purpose of densification would be undesirable, as formation of the LP-TEOS layer at such a high temperature of 700C- 800C, as claimed in claim 1 would result in the penetration of carbon into adjacent active regions of the device. Remarks related to the issue were previously provided by the applicants in the Amendment After Final, filed on December 20, 2002, at page 5, paragraph 3:

The Applicants note that in the TEOS process, carbon introduced in the source material tetraethosiloxane,  $\text{Si}(\text{OC}_2\text{H}_5)_4$  has a high degree of penetration into the active area at the high temperature of “not less than 650C” stated in Shin. Such penetration of carbon into the active area results in degrading of the characteristics of the resulting semiconductor device, as is well known in the art. In view of this, the TEOS process is generally performed at a low temperature for formation of device isolation structures, and therefore, TEOS is not an acceptable replacement for the HTO process as claimed in the present invention.

In view of the above, it is submitted that the LP-TEOS process is unsuitable for densification of the underlying insulating layer in connection with the present invention, and therefore, for purposes of the present invention, does not represent an “art equivalent” of the HTO layer claimed in claim 1 of the present invention.

It is therefore submitted that the combination of the Laparra, Park, and Shin references fails to teach or suggest the present invention as claimed in independent claim 1. In particular, none of the references, alone, or in combination, teach or suggest “providing a high-temperature oxide (HTO) layer on the insulating layer using a silane-based source gas” as claimed. It is believed that claim 1 as amended above clearly distinguishes the claimed HTO step from the LP-TEOS step, a step that is suggested in the Office Action as being an “art equivalent” of HTO.

Accordingly, reconsideration of the rejection and allowance of claim 1 are respectfully requested. With regard to the various dependent claims 2 and 4-13, it follows that these claims should inherit the allowability of the independent claim from which they depend.

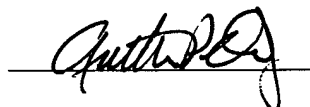
Closing Remarks

It is submitted that all claims are in condition for allowance, and such allowance is respectfully requested. If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Respectfully submitted,

Date: December 19, 2003

Mills & Onello, LLP  
Eleven Beacon Street, Suite 605  
Boston, MA 02108  
Telephone: (617) 994-4900, Ext. 4902  
Facsimile: (617) 742-7774  
J:\SAM\0167\167amendment2.wpd

  
Anthony P. Onello, Jr.  
Registration Number 38,572  
Attorney for Applicant

A COMPARISON OF PLANARIZATION PROPERTIES  
OF TEOS AND SiH<sub>4</sub> PECVD OXIDES

Chris G. Magnella and Tammy Ingwersen  
Harris Corporation  
Melbourne, Florida 32901

Earl Fleck  
ASM America, Inc.  
Phoenix, Arizona 85040

TECHNOLOGY CENTER 2800

DEC 31 2003

RECEIVED

ABSTRACT

TEOS and SiH<sub>4</sub> PECVD films were deposited over patterned polysilicon in a parallel plate batch reactor. Both films were then etched using an etch-back planarization process. Deposition and etch uniformity and quality were compared using optical thickness measurements and SEM cross sections. Electrical yield was also calculated for contact strings using each type of oxide. Nitrous oxide and oxygen were compared as reactants with TEOS. The use of O<sub>2</sub> gave the best TEOS product wafer deposition uniformity, 13.3 % (3 sigma). Overall uniformity for SiH<sub>4</sub> PECVD product wafers was 15.5 % (3 sigma). Etch uniformity was 5.0 % (3 sigma) for TEOS compared to 17.0 % (3 sigma) for SiH<sub>4</sub> films. TEOS step coverage before and after the etch was superior to SiH<sub>4</sub>. Dilute HF acid exposed seams in SiH<sub>4</sub> films, whereas TEOS films were unaffected. Refractive index and etch rate did not change after a 30 minute, 450 C anneal.

INTRODUCTION

As geometries of polysilicon and metal conductor lines decrease, step coverage requirements of dielectric films become more demanding. The dielectric must be able to cover steps without cusping so that subsequent planarization processes will leave a surface free from grooves that can cause interlevel and intralevel electrical shorts. Because planarization requires multiple processing steps, it is subject to the effects of cumulative process variation. This paper addresses some of the problems associated with the deposition and planarization of silane based PECVD oxides and the solutions offered by TEOS based PECVD films.

Cusping is the greatest problem with silane PECVD oxides. CVD silane deposition above 600 C is typically very conformal, with only small cusping problems (1). This is due mostly to the rapid surface migration generated by elevated processing temperatures and lower process pressures, which creates a larger mean free path and thus

June 13-14, 1988 V-MIC Conf.

CH-2624-5/88/0000-0366 \$01.00 C 1988 IEEE



allow more angles of arrival for reactants. Surface migration is limited in lower temperature PECVD depositions (335 C in this work), which causes increased cusping. PECVD is deposited at much higher pressures, thus reducing the mean free path and the possible angles of arrival of reactants (6). As geometry aspect ratios increase, cusping leads to the formation of caverns between lines during deposition which are opened when the film is planarized.

The addition of phosphorus to PECVD films reduces the cusping by lowering the energy needed for atom migration. Phosphorus, however, changes the etch rate of the PECVD drastically. In this work, a 5 w% phosphorus film changed the PECVD etch rate by a factor of two. Non-uniformities in the film cause large variations in the film after planarization. In this work, the phosphorus range was 0.8 w%, which resulted in an etch uniformity of 24 % (3 sigma). These variations across the wafer can leave devices with very thin dielectric layers that can cause shorts or degrade device reliability.

Phosphorus doped PECVD films create another etch problem. As the deposition fills spaces, a seam forms where the oxide sidewalls meet. This seam has been found to etch at a much higher rate than the bulk. SIMS analysis shows that this film is phosphorus rich. The seam oxide may be a degenerate SiO<sub>x</sub> since reactants and byproducts cannot reach the bottom of the seam as easily as the bulk. The planarization process will etch these areas faster, leaving large grooves in the oxide.

A final problem with silane PECVD is gas phase nucleation. Under normal circumstances, the SiO<sub>2</sub> is formed at the wafer surface. If the RF field is too great, the dissociated gas molecules will react in the gas stream and shower onto the wafer (2). The resulting embedded particles cause large local differences in oxide thickness, which interfere with photoresist coat and exposure (Figures 1a,b ).

#### EXPERIMENTAL

Two micron SiH<sub>4</sub> and TEOS PECVD films were deposited in an ASM Plasma III reactor. The TEOS films were deposited at ASM Inc., using a parallel disk boat. The TEOS flow was controlled using a MKS1150 TEOS flow controller. The SiH<sub>4</sub> PECVD films were deposited in-house using a standard production process on parallel plate boats. Table 1 lists TEOS and SiH<sub>4</sub> processing conditions.

The films were deposited at the polysilicon-metal 1 dielectric step in a 1.25 um CMOS process. Six batches of 25 device wafers were processed with TEOS oxide. Bare silicon pilots were processed with each batch. A Nanometrics Nanospec AFT was used to measure all oxide

thicknesses. Pre and post deposition measurements were used to determine oxide thickness on product. SEM's were taken to evaluate deposition conformality. Two of the batches were split between TEOS and SiH<sub>4</sub> oxide. These splits were re-combined and processed through Metal 1 for electrical contact probe results. In addition film analysis was done to further characterize the TEOS film.

Using an RIE hexode etcher, TEOS etch rates and selectivities were adjusted until they were identical to the standard PECVD planarization etch parameters. Batches of 6 wafers for TEOS and SiH<sub>4</sub> films were processed in order to determine wafer-to-wafer, within-wafer and run-to-run uniformity. Pre and post etch Nanospec measurements were used to determine etch uniformity. SEM cross sections were taken to evaluate the planarity of the etch.

The planarization etch used was a 5 step process. Step 1 was a high selectivity (> 4:1) C.D. cut. Step 2 was used to taper the contact. In step 3, the bulk of the planarization takes place. Step 4 uses O<sub>2</sub> to burn off any remaining photoresist from planarization. Step 5 is another highly selective etch used to clean up non-uniformities in the oxide (4). This step is critical since severe non-uniformities will cause some areas to be overetched. This overetch may remove the metal polysilicon shunt exposed in the bottom of the contact and cause high contact resistance.

## RESULTS

### DEPOSITION UNIFORMITY:

The within-wafer and wafer-to-wafer uniformities for TEOS and SiH<sub>4</sub> PECVD are listed in Table 2. The first 3 TEOS batches were processed using N<sub>2</sub>O and TEOS. The overall wafer-to-wafer uniformity (3 sigma average of all points in 3 runs) was 19.2 % versus 15.2 % for PECVD. When O<sub>2</sub> was substituted for N<sub>2</sub>O on the last 3 batches the wafer-to-wafer uniformity improved to 6.0 %. The overall within-wafer uniformity for TEOS reacted with N<sub>2</sub>O was slightly worse than the standard PECVD; 8.2 % versus 6.0 %. TEOS reacted with O<sub>2</sub> improved within-wafer uniformity to 4.0 %.

### DEPOSITION QUALITY:

The PECVD films had cusping problems as expected. When exposed to dilute HF, the oxide seam became visible (Figure 2). The TEOS films did not show any cusping problems, and dilute HF did not highlight any seams (Figure 3). The top and bottom of the step are approximately the same thickness and the sidewall oxide is nearly vertical. The TEOS molecule retains enough energy after dissociation to migrate down sidewalls. Lower deposition pressure increases the mean free path for migration resulting in better step coverage.

Embedded particles in the TEOS films were not formally compared since the TEOS was processed at ASM America Inc. in a non-clean room environment. Ideally, TEOS oxide should be better than SiH<sub>4</sub> oxide because TEOS is not pyrophoric. Thus, particulate sometimes seen with SiH<sub>4</sub> films due to gas phase nucleation would not be a problem with TEOS.

#### ETCH UNIFORMITY:

Etch uniformity was drastically improved with TEOS oxide (Table 2) because there is no phosphorus in the film and there is no evidence of a degenerate oxide between lines. Overall wafer-to-wafer etch uniformity (3 sigma average of all points measured) was reduced from 8.6 % to 4.4 %. Overall within-wafer uniformity was reduced to 2.5 % from 14.1 %

The range of the amount of oxide etched across a wafer decreased 250 % when TEOS was used in place of SiH<sub>4</sub> PECVD. This significantly reduces the chance of severe overetch during processing. TEOS reacted with N<sub>2</sub>O reduced the overall planarization etch process (deposition, photoresist, etch) by 30 % (Table 2) within a wafer and by 8 % wafer-to-wafer. Work on TEOS reacted with O<sub>2</sub> is not yet complete, but should produce similar results.

#### ETCH QUALITY:

Cross sections of TEOS films were also superior to silane PECVD. Figures 4,5 show the caverns formed when PECVD is etched and the smooth bottom after TEOS etch on the most severe topography. On less severe topography, TEOS gives a much smoother post-etch surface (Fig 6,7). Note that the PECVD film leaves grooves in minimum spaced lines; TEOS does not.

#### OTHER FILM CHARACTERISTICS:

The TEOS film was annealed at 450 C for 30 minutes in forming gas. No changes in etch rate or refractive index were found. The only parameter having an effect on refractive index was the replacement of N<sub>2</sub>O with O<sub>2</sub>. The R.I. for unannealed TEOS using N<sub>2</sub>O was approximately 1.51; substituting O<sub>2</sub> changed the R.I. to approximately 1.47. The standard SiH<sub>4</sub> PECVD R.I. is approximately 1.48

SIMS and ESCA analysis indicate that mobile ion concentrations in both oxides are about equal (Figures 8a,b). FTIR analysis shows that the TEOS film has more oxidation states than the PECVD film.

TEOS film stress was found to be a function of process pressure. The stress was compressive (~2.0 - 3.0 x 10E09 dynes/cm<sup>2</sup>) at 250 mTorr. At 750 mTorr the film appeared slightly compressive or tensile, but at 1000 mTorr the film stress was tensile (~1.5 - 2.5 x 10E09 dynes/cm<sup>2</sup>). Process pressure was maintained below 750 mTorr and

optimized for deposition uniformity.

#### ELECTRICAL PROBE RESULTS:

Contact yields were measured on a 1000 contact string device. Interlevel shorts were tested on a Metal 1 - polysilicon serpentine structure. Metal 1 - Metal 1 shorts were measured on a meander structure. No statistically significant difference existed between the TEOS and SiH<sub>4</sub> films to a 90 % confidence level for any of the tests.

#### CONCLUSIONS

Deposition and planarization properties of PECVD TEOS oxide were compared to those of silane based PECVD oxide. TEOS oxide exhibited better step coverage and did not have a degenerate oxide seams that were affected by dilute HF. TEOS films do not require phosphorus doping for step coverage, thus have very uniform etch rates. Etch uniformity was improved 550 % within-a-wafer and 200 % wafer-to-wafer using TEOS oxide. Electrical contact yields, interlevel and intralevel shorts using TEOS were equal to PECVD films. TEOS was easily retrofitted to the ASM deposition system

#### ACKNOWLEDGEMENTS

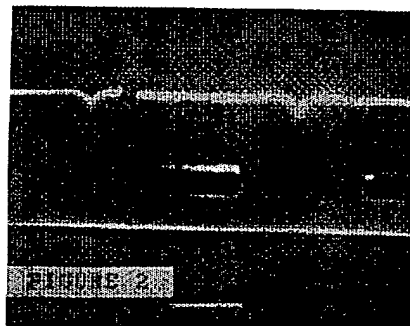
The authors would like to thank the following individuals and organizations for their contributions to this work: Jim Rauchfuss and George Mraz for SEM analysis, Jack Linn for ESCA and FTIR analysis, and ASM America and Harris VHSIC Operation for their support during the entire project.

#### REFERENCES

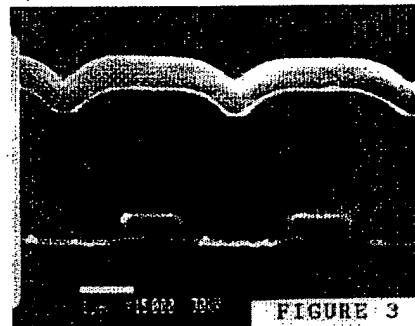
1. F.S. Becker, et al., J. Vac Sci Tech. B 5 1555 (Nov/Dec 1987).
2. F.S. Becker, et al., J. Vac Sci Tech. 732 (Feb 1987).
3. R.H. Dorrance, et al., J. Vac Sci Tech. B 5 1564 (Nov/Dec 1987).
4. G. Gimpleson, C. Russo, 1984 V-MIC Conference Proceedings, pp. 37, IEEE, Santa Clara CA.
5. R.M. Levin, K. Evans-Lutterudt, et al., J. Vac Sci, vol B1, p 54 (1983).
6. S. Wolf, R.N. Tauber, Silicon Processing For the VLSI Era, Vol 1 - Processing Technology, Lattice Press, Sunset Beach, CA, 1986.



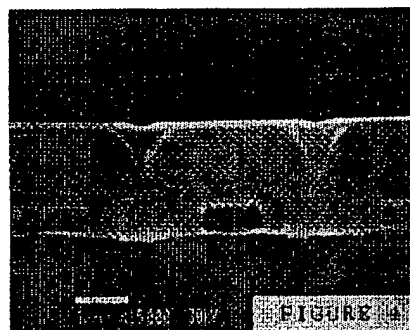
# EMBEDDED PARTICLES



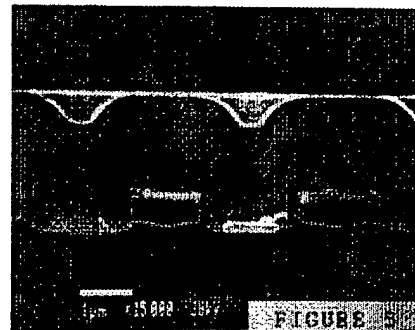
PECVD FILM EXPOSED  
TO DILUTE HF  
(SEAMS)



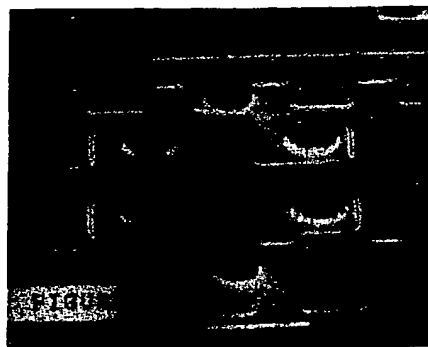
TEOS FILM EXPOSED  
TO DILUTE HF  
(NO SEAMS)



POST PLANARIZATION  
(PECVD CAVERNS)



POST PLANARIZATION  
(TEOS)



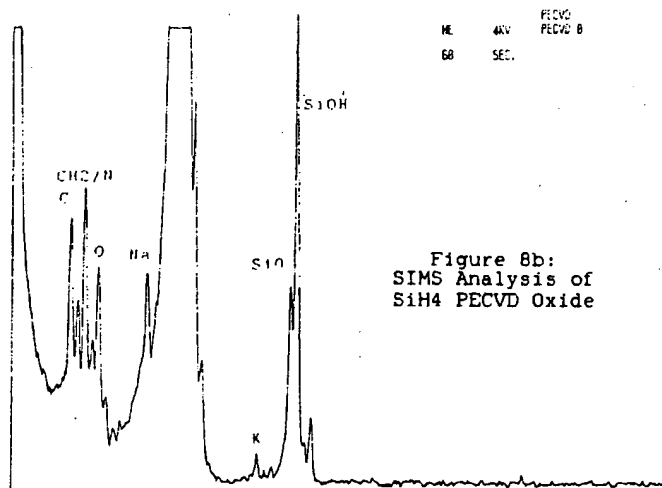
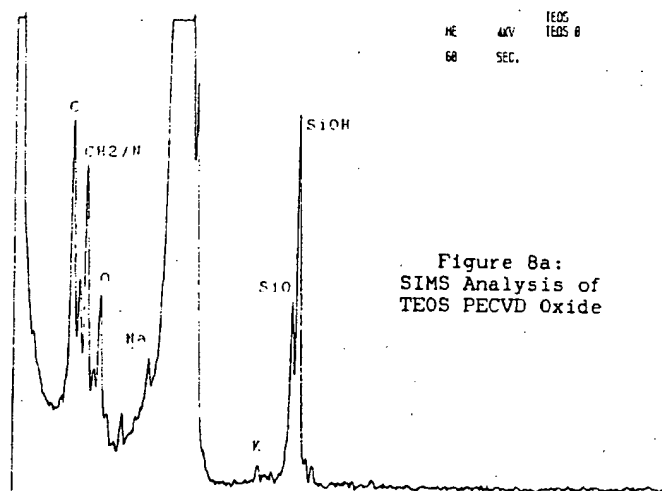
NOTE THAT THE PECVD FILM (FIG. 7)  
LEAVES GROOVES IN MINIMUM SPACED  
LINES; TEOS DOES NOT (FIG 6)

TABLE 1  
TEOS AND SIH<sub>4</sub> OXIDE PROCESSING CONDITIONS

PARAMETER	SIH <sub>4</sub>	TEOS (O <sub>2</sub> )	TEOS (N <sub>2</sub> O)
SIH <sub>4</sub> /TEOS FLOW (SCCM)	120	175	200
AR (SCCM)	---	1125	---
O <sub>2</sub> (SCCM)	---	700	100
N <sub>2</sub> O (SCCM)	4000	---	2000
TEMP (DEGREE C)	335	300	300
PRESSURE (MTORR)	1250	400	400
POWER (PEAK KW)	1.8	1.75	2.25

TABLE 2  
PECVD FILM COMPARISON

PROPERTY	SIH <sub>4</sub>	TEOS (N <sub>2</sub> O)	TEOS (O <sub>2</sub> )
AVG WAFER/ WAFER UNIFORMITY (PRODUCT)	15.2%	19.2%	6.0%
AVG WITHIN WAFER UNIFORMITY (PRODUCT)	6.0%	8.2%	4.0%
AVG WAFER/ WAFER UNIFORMITY (ETCH)	8.6%	4.4%	
AVG WITHIN WAFER UNIFORMITY (ETCH)	14.1%	2.5%	
OVERALL ETCH WITHIN WAFER UNIFORMITY	23.6%	16.5%	
OVERALL ETCH WAFER-TO-WAFER UNIFORMITY	33.8%	31.1%	



## STICKING COEFFICIENT AS A SINGLE PARAMETER TO CHARACTERIZE STEP COVERAGE OF SiO<sub>2</sub> PROCESSES

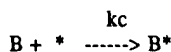
Lie-Yea Cheng, Juan, C. Rey, James P. McVittie and Krishna C. Saraswat  
*Center for Integrated Systems, Stanford University, Stanford, CA 94305*

### SUMMARY

We use a single parameter, the sticking coefficient (or reaction probability) to model the step coverage of low pressure chemical vapor deposited (LPCVD) SiO<sub>2</sub> films. Earlier studies (1,2) show that a low sticking coefficient, instead of surface diffusion, is the key step coverage improving mechanism. A simulation program based on a hypothesized reaction mechanism has been written to simulate deposition profiles. The program is capable of simulating redeposition and surface diffusion. Simulated profiles, using a single sticking coefficient (SC), agree well with experimental oxide films deposited on a variety of different geometries. The coefficient depends strongly on the silicon source used, and its magnitude decreases with increasing temperature.

### EXTENDED ABSTRACT

In previous studies(1,2), we have used a test structure with an overhang feature (shown in Figure 1(a)) to separate the step coverage improving mass transport mechanisms at the surface. The improving mechanisms include surface diffusion and reemission, which is due to a low sticking coefficient of reacting species. We observed the deposition profiles under the overhang vary with cavity height, which can only be explained by reemission effect. The constant thickness of the oxide films above the overhang indicates that surface diffusion plays a minor role in improving step coverage. If surface diffusion played a major role, we would expect the oxide thickness to decrease near the cavity. With these two observation, we conclude that reemission due to a low sticking coefficient of reacting species is the major step coverage improving mechanism. A ballistic Monte Carlo program has been written to simulate the oxide deposition profiles on the test structure. The simulation is based on the assumption that the deposition of a precursor species is the rate controlling step. We assume an Eley-Rideal surface reaction mechanism as shown below in which A is the precursor species and B is the other species that A has to react to form the film.



kc : conversion rate constant  
\* : reactive site on surface



From the subsequent rate equations, we can derive SC as :

$$SC = \frac{\text{growth rate}}{\Gamma_A} = \frac{kr ka N}{kd + kr + ka \Gamma_A \{1 + kr/(kc \Gamma_B)\}}$$

$N$  : number of reactive site per unit area  
 $\Gamma_A$  : flux of A (precursor)  
 $\Gamma_B$  : flux of B

Assume  $ka \Gamma_A \{1 + kr/(kc \Gamma_B)\} \ll kd + kr$ , then

$$SC \sim \frac{kr ka N}{kd + kr}$$

The assumption that  $ka \Gamma_A \{1 + kr/(kc \Gamma_B)\} \ll kd + kr$  holds when the precursor flux ( $\Gamma_A$ ) is very low, which is reaffirmed by Watanabe et al.'s research (4). Under these assumptions, SC is only a function of temperature and is independent of flux; therefore, we can use a constant value to simulate deposition on different geometries. In the simulator, particles are randomly dropped from a certain distance above the surface. They can either get adsorbed at the surface or desorb to reach other surfaces. Surface diffusion simulation starts when particles are adsorbed at the surface. The simulator is detailed in the companion paper (3).

The simulated results match very well with experimental results by merely considering reemission effect (low sticking coefficient) without any surface diffusion. The silicon sources investigated included silane, diethylsilane (DES), tetraethoxysilane (TEOS), and tetramethylcyclotetrasiloxane (TMCTS). For low pressure deposition (< 800 mtorr), the sticking coefficients required to match the experimental results for silane, DES, TEOS, and TMCTS are 0.26, 0.1, 0.045, and 0.04 respectively. This shows the strong dependence of SC on silicon sources.

Simulated profiles on test structures and trenches fit deposition profiles very well by using a single sticking coefficient. In Figure 1, we compare the DES oxide deposition (410°C, 750 mtorr) and simulated profiles (SC = 0.1). A plot of thickness ratio vs. aspect ratio for deposited(also DES source under same condition) and simulated trenches is shown in Figure2. The close fit indicates that sticking coefficient is an effective process characterizing parameter. This parameter, from the reaction mechanism, is affected by temperature. We studied this effect for silane and DES sources. The temperature ranges for the silane and DES sources are 370°C - 430°C, and 380°C - 440°C respectively. In both cases, sticking coefficient decreases with temperature. Watanabe et al. (4) also observed the same trend for their study of silane source oxide deposition. Sticking coefficients obtained in the two independent studies agree very

agree very well in their temperature dependence (see figure 3). Since SC is inversely proportional to  $k_d$  (desorption rate constant), this suggests that the increased temperature increases the desorption rate.

#### ACKNOWLEDGEMENT

The research is jointly supported by SRC and DARPA.

#### REFERENCES

- (1) L.-Y. Cheng, J. P. McVittie and K. C. Saraswat; 2nd Int. Symp. on ULSI Sci. and Tech.; The Electrochemical Society; Vol 89; LA, CA, 1989.
- (2) L.-Y. Cheng, J. P. McVittie and K. C. Saraswat; submitted to APL; Jan 1990.
- (3) J. C. Rey, L.-Y. Cheng, J. P. McVittie and K. C. Saraswat, "Numerical Simulation of CVD Trench Filling Using A Surface Reaction Coefficient Model", this VMIC poster.
- (4) K. Watanabe, and H. Komiyama, J. Electrochem. Soc., Vol 137, 1222, 1990.

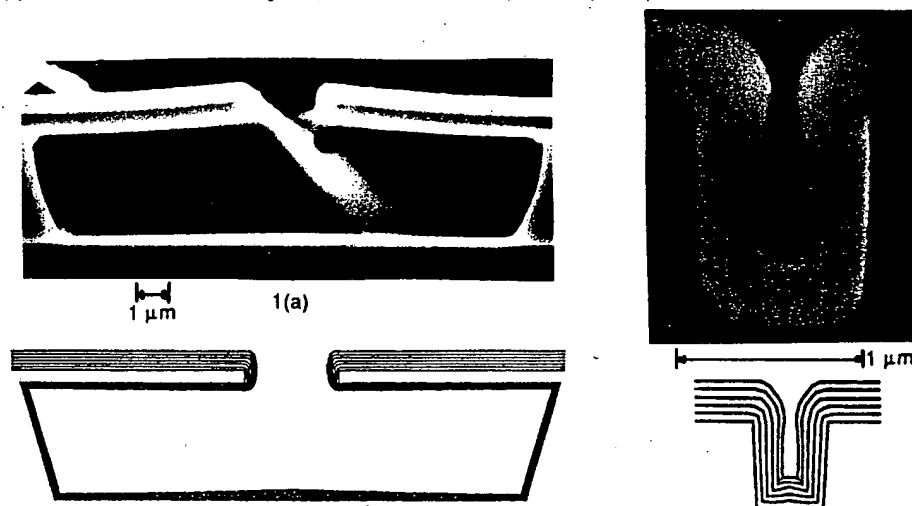


Figure 1. Comparison of DES source oxide deposition and simulated (SC=0.1) profile on the test structure and trench with aspect ratio equal to 1.187

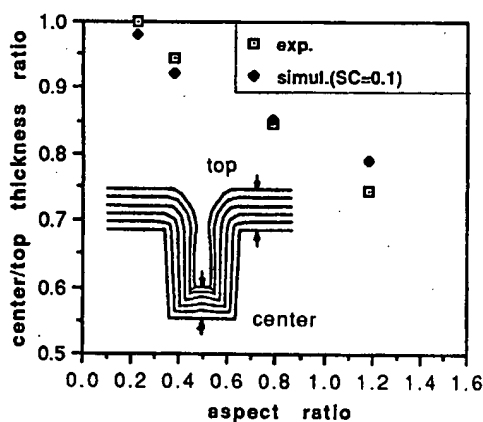


Figure 2. Thickness ratio of deposited and simulated trench profiles vs. trench aspect ratio. (DES source)

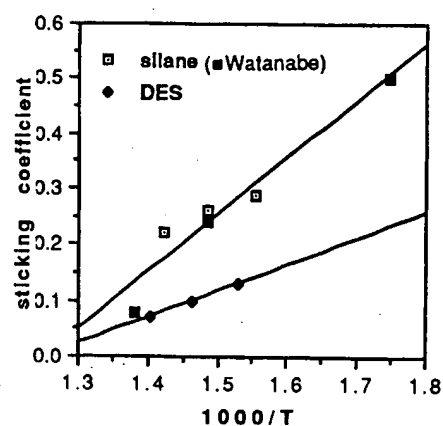


Figure 3. Temperature dependence of sticking coefficient (SC) for silane (including Watanabe et al.'s data) and DES source.